

Westinghouse P-50 Computer Repertoire of Instructions

Reconstructed and typeset from the original manual scan.

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1 Command Structure

All P-50 instructions may be either directly or indirectly addressed. The bit configuration for each address mode is as follows.

Instruction, Direct Address Mode

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Function Code					0	Relative Address								Content

In the direct address mode, the 14-bit operand address required to reference a memory cell is generated by the six most significant bits of the program address register and the low-order eight bits of the instruction (the relative address). This imposes the requirement that all instructions which are directly addressed have their operand in the same block of 256 words in which the instruction is located.

Instruction, Indirect Address Mode

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Function Code					1	Relative Address								Content

Address Defined by P Register and Relative Address

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Operand Address														Content

In the indirect address mode, the operand address is defined by the contents of the location specified by the six most significant bits of the P Register and the low-order eight bits of the instruction (the relative address).

Input/Output instructions vary slightly from this pattern.

Input/Output Instruction, Direct Address Mode

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Function Code					0	Not Used	Channel Number							Content

In the direct address mode, used primarily for input, the low-order six bits of the instruction designate the I/O channel.

Input/Output Instruction, Indirect Address Mode

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Function Code					1	Relative Address								Content

Address Defined by P Register and Relative Address (I/O)

13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Not Used		Word Select						Channel Number						Content

In the indirect address mode, used mainly for output, the six most significant bits of the program address register and the low-order eight bits of the instruction specify the location of the I/O data word. The I/O data word contains the channel number in the low-order six bits (5–0) and the word number relative to the channel in bits 11–6.

Timing

The execution of an instruction in the indirect mode occupies 4.5 microseconds more than when the instruction is executed in the direct mode.

2 Description of Operation

The table below summarizes every instruction in the P-50 repertoire: its register-transfer expression, mnemonic, octal operation code, whether it affects the designators (SET) or belongs to the control-transfer class (K), and a brief remark. Full descriptions of every instruction follow in Section 3.

Inst.	Mne	Code	Des	Remarks
$A + (Y) \rightarrow A$	ADD	10	SET	Add
$A - (Y) \rightarrow A$	SUB	11	SET	Subtract
$(Y) \rightarrow A$	ENL	32, 33	SET	Load A
$A \rightarrow (Y)$	STL	37	SET	Store A
$A \oplus (Y) \rightarrow A$	EOR	13	SET	Selective complement
$L(A)(Y) \rightarrow A$	AND	12	SET	Logical product of (A) & (Y)
$(Y) R1 \rightarrow (Y)$	RSH	16, 17	SET	End-off, sign extend
$(Y) L1 \rightarrow (Y)$	LSH	14, 15	SET	End-around
$(Y) - 1 \rightarrow (Y)$	DCR	01	SET	Decrement
SET $(Y)_{13}$	SMB	03	SET	Set most significant bit
CLR $(Y)_{13}$	CMB	02	SET	Clear most significant bit
$(Y_{4-0}) \rightarrow DES$	EDR	05		Load designators
$DES \rightarrow (Y_{4-0})$	SDR	06, 07	K	Store designators
$I/O \rightarrow A$	INT	30, 31	SET	Input
$A \rightarrow I/O$	OUT	34, 35	SET	Output
$Y \rightarrow P$	JMP	24	K	Jump
$Y \rightarrow P$	SLJ	22	K	Set lockout
$Y \rightarrow P$	CLJ	23	K	Clear lockout
$Y \rightarrow P$ if 0 desig. set	ZJP	20	K	Jump on zero
$Y \rightarrow P$ if pos. desig. set	PJP	27	K	Jump on positive
$Y \rightarrow P$ if even desig. set	EJP	21	K	Jump on even
$Y \rightarrow P$ if EAC desig. set	CJP	25	K	Jump on end-around carry
$Y \rightarrow P$ if overfl. desig. set	OJP	26	K	Jump on overflow
$(P) \rightarrow Y, Y \rightarrow P$	RJP	36	K	Return jump
Stop	STP	00, 04	K	Stop

3 Repertoire of Instructions

Instructions are presented below in order of increasing octal operation code. Each entry gives the mnemonic, the octal code, execution time, and a full description of the instruction's effect, including its influence on the five designators (Even, Zero, Positive, Overflow, and End-Around Carry).

In each entry's descriptive title, the letters that combine to form the mnemonic are underlined at the position where they occur — for example, Decrement for DCR, or Input to Computer for INT.

STP (octal 00, 04)

Stop

Execution time: 9 microseconds

The computer comes to a stop with the contents of bits 13–8 of the P Register in bits 13–8 of the S Register and the contents of bits 7–0 of the stop instruction in bits 7–0 of the S Register. The mode bit is disregarded and the designators are unchanged.

DCR (octal 01)

Decrement

Execution time: 13.5 microseconds

A negative one is added to the operand. The appropriate designators are set if an overflow, end-around carry, zero, positive number, and/or even number results; otherwise, all the designators are cleared except the overflow designator.

CMB (octal 02)

Clear Most Significant Bit

Execution time: 13.5 microseconds

The sign bit (bit 13) of the operand is cleared to zero and the positive designator is set. The zero and even designators are set or cleared depending on the resultant contents of the operand. The end-around carry designator is cleared, and the overflow designator is unchanged.

SMB (octal 03)

Set Most Significant Bit

Execution time: 13.5 microseconds

The sign bit (bit 13) of the operand is set to one. The even and zero designators are set or cleared depending on the resultant contents of the operand. The positive and end-around carry designators are cleared, and the overflow designator is unchanged.

EDR (octal 05)

Enter Designators

Execution time: 13.5 microseconds

Bits 0–4 of the operand replace the contents of the five designators in the following manner:

Bit 4	→	Even designator
Bit 3	→	Zero designator
Bit 2	→	Positive designator
Bit 1	→	Overflow designator
Bit 0	→	End-around carry designator

Only this instruction can clear the overflow designator once it has been set.

SDR (octal 06, 07)**Store Designators***Execution time: 13.5 microseconds*

The five designators are stored in bits 0–4 of the operand. The designators are not changed as a result of this instruction. The storage is as follows:

Even designator	→ Bit 4
Zero designator	→ Bit 3
Positive designator	→ Bit 2
Overflow designator	→ Bit 1
End-around carry designator	→ Bit 0

(Y)_{5–13} are cleared to zero.

ADD (octal 10)**Add Accumulator***Execution time: 18.0 microseconds*

The operand is added to the contents of the accumulator and the result is left in the accumulator. The result is positive zero only if the initial contents of the accumulator and of the operand were both positive zero. The even, zero, positive, and end-around carry designators are set or cleared by the execution of this instruction. The overflow designator will be set if an overflow occurs; otherwise it is unchanged.

SUB (octal 11)**Subtract Accumulator***Execution time: 18.0 microseconds*

The operand is complemented and added to the contents of the accumulator (a subtraction, in effect); the result is left in the accumulator. The difference is positive zero only if the initial contents of the accumulator were positive zero and the operand was negative zero. The even, zero, positive, and end-around carry designators are set or cleared by the execution of this instruction. The overflow designator will be set if an overflow occurs; otherwise, it is unchanged.

AND (octal 12)**Logical AND***Execution time: 18.0 microseconds*

For any bit position of the operand which contains a zero, the corresponding bit position of the accumulator is unconditionally set to zero; all other bit positions of the accumulator remain undisturbed. The effect of this instruction is to compute the bit-by-bit, or logical, product of the contents of the accumulator and the operand, leaving the result in the accumulator. The even, zero, and positive designators are set or cleared depending on the result in the accumulator. The end-around carry designator is set; the overflow designator is unchanged.

Example:

	(Accumulator)	(Operand)
Initially:	01011	00101
After execution of AND instruction:	00001	00101

(Positive designator is set to one; even and zero designators are cleared to zero, and the EAC is set to one.)

EOR (octal 13)**Exclusive OR***Execution time: 18.0 microseconds*

For any bit position of the operand which contains a one, the corresponding bit of the accumulator is complemented; all other bit positions of the accumulator remain undisturbed. The even, zero, and positive designators are set or cleared depending on the result in the accumulator. The end-around carry designator is cleared, and the overflow designator is unchanged.

Example:

	(Accumulator)	(Operand)
Initially:	01011	00101
After execution of EOR instruction:	01110	00101

(Even and positive designators are set to one; end-around carry and zero designators are cleared to zero.)

LSH (octal 14, 15)**Left Shift***Execution time: 18.0 microseconds*

Shift the operand to the left one bit position; the high-order bit replaces the low-order bit of the operand. The even, zero, end-around carry, and positive designators are set or cleared depending on the result. The overflow designator is set if the sign of the operand changed as a result of the left shift; otherwise it is unchanged.

For example, the operand = 24505. After LSH, the operand = 11213 with the positive, end-around carry, and overflow designators set to one, all other designators cleared to zero.

RSH (octal 16, 17)**Right Shift***Execution time: 18.0 microseconds*

Shift the operand to the right one bit position; the high-order bit is replaced by the original sign bit. Note that this is an end-off shift and that the low-order bit enters the end-around carry designator. The zero, even, and positive designators are set or cleared depending on the result. The overflow designator is unchanged.

For example, the operand = 24505. After RSH, the operand = 32242 with the end-around carry designator set to one, the positive, zero, and even designators cleared to zero.

ZJP (octal 20)**Zero Jump***Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump*

If the zero designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. Note that the zero designator will be set by negative zero (all ones) or by positive zero (all zeros). The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.^a

^aNote that when an operand address is transferred to the P Register, the instruction at location operand address plus one is the next instruction to be executed.

EJP (octal 21)**Even Jump***Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump*

If the even designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. Note that the even designator is set whenever bit 13 and bit 0 of a referenced location are equal. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

SLJ (octal 22)**Set Lockout and Jump***Execution time: 13.5 microseconds*

Lock out all interrupts and transfer the operand address to the P Register. The designators are not changed as a result of this instruction.

CLJ (octal 23)**Clear Lockout and Jump***Execution time: 13.5 microseconds*

Remove the interrupt lockout and transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following execution of this instruction.

JMP (octal 24)**Jump***Execution time: 13.5 microseconds*

Unconditionally transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

CJP (octal 25)**End-Around Carry Jump***Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump*

If the end-around carry designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

OJP (octal 26)**Overflow Jump***Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump*

If the overflow designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

PJP (octal 27)**Positive Jump***Execution time: 13.5 microseconds if jump, 9.0 microseconds if no jump*

If the positive designator is set, transfer the operand address to the P Register. Otherwise, take the next instruction. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

INT (octal 30, 31)**Input to Computer***Execution time: 18.0 microseconds*

In the direct mode, data on the input channel specified by bits 0–5 of the instruction are input into the accumulator. In the indirect mode, bits 0–5 of the I/O data word select the input channel and bits 6–11 the word address. The indirect mode should be used with utmost caution; otherwise, conflict with other peripheral devices may occur. The designators are set, cleared, or unchanged as in the ENL instruction.

ENL (octal 32, 33)**Enter Accumulator***Execution time: 18.0 microseconds*

Clear the accumulator, then transmit the operand to the accumulator. The even, zero, and positive designators are set or cleared depending on the resultant contents of the accumulator. The end-around carry designator is cleared to zero, and the overflow designator is unchanged.

OUT (octal 34, 35)**Output from Computer***Execution time: 18.0 microseconds*

If indirectly addressed, the contents of the accumulator are output on the channel selected by bits 0–5 of the I/O data word and the word selected by bits 6–11. In the direct mode, the contents of the accumulator are output on the channel selected by bits 0–5 of the instruction. The designators are set, cleared, or unchanged as in the STL instruction.

RJP (octal 36)**Return Jump***Execution time: 22.5 microseconds*

Store the contents of the P Register in the operand; transfer the operand address to the P Register. The designators are not changed as a result of this instruction. Interrupt is inhibited immediately following the execution of this instruction.

STL (octal 37)**Store Accumulator***Execution time: 18.0 microseconds*

Store the contents of the accumulator in the operand. The even, zero, and positive designators are set or cleared, depending on the contents of the accumulator. The end-around carry designator is cleared to zero, and the overflow designator is unchanged.

4 The Designators

Even Designator

The even designator is affected (set or cleared) by the execution of the following instructions: DCR, CMB, SMB, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL.

When the even designator is set by the execution of an instruction other than EDR, it implies that bits 0 and 13 of the result of the instruction are both zero or both one.

Zero Designator

The zero designator is affected (set or cleared) by the execution of the following instructions: DCR, CMB, SMB, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL.

When the zero designator is set by the execution of an instruction other than EDR, it implies that the result of the instruction is 00000 or 37777.

Positive Designator

The positive designator is affected (set or cleared) by the execution of the following instructions: DCR, EDR, ADD, SUB, AND, EOR, LSH, RSH, INT, ENL, OUT, STL. The positive designator is always set by the execution of the CMB instruction, and always cleared by the execution of the SMB instruction.

When the positive designator is set by the execution of an instruction other than EDR, it implies that bit 13 of the result of the instruction is zero.

End-Around Carry Designator

The end-around carry designator is affected (set or cleared) by the execution of the following instructions: DCR, EDR, ADD, SUB, LSH, RSH. The end-around carry designator is always cleared when CMB, SMB, EOR, INT, ENL, OUT, and STL instructions are executed. EAC is always set with execution of AND.

When the end-around carry designator is set by the execution of a DCR, ADD, SUB, or LSH instruction, it implies that an end-around carry has occurred. When the end-around carry designator is set by the execution of an RSH instruction, it means that the low-order bit of the operand which is shifted off is a one.

Overflow Designator

The overflow designator is set whenever two positive numbers are summed and the result is negative, or two negative numbers are summed and the result is positive. The overflow designator can be set by the execution of the following instructions: DCR, ADD, SUB, LSH. The EDR instruction only can be used to clear the overflow designator.

Designators When Clear

The designators, when clear, indicate the following:

Designator	Meaning when clear
Even designator	Odd
Zero designator	Non-zero
Positive designator	Negative
End-around carry designator	No end-around carry
Overflow designator	No overflow