

VARIAN 620/L QUICK REFERENCE CARD

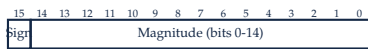
Processor Architecture & Addressing

Registers

Reg	Bits	Purpose
A	16	Accumulator: arithmetic/logical results
B	16	Extends A in MUL/DIV; second index register
X	16	Index register
P	15	Program counter: address of the next fetch
U	16	Instruction register (holds the fetched word; visible in STEP mode)
OF	1	Overflow indicator
SS1-3	1 ea	Sense switches (front panel); tested by JSSn/XSn

Memory: 4K to 32K in 4K modules; addresses wrap modulo the installed size. Only A, B, X are directly accessible to the programmer.

Data Word Format



Negative numbers in 2's complement. Logical data in true (unsigned) form.

Indirect-Address Word



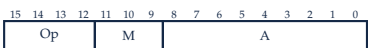
I=0: this word holds the operand's address. I=1: it holds the address of *another* indirect word. Any number of levels; each adds one machine cycle (1.8 μ s).

Instruction Word Formats

Single-word addressing (op 01-07, 11-17)



Non-addressing (shift, register change, control, I/O)



Op=00: M selects shift (4), register change (5), or control (7). Op=10 (I/O): M selects the I/O subgroup; see the back page.

Double-word: Jump / Mark / Execute (op 00, M=1/2/3)

First word:



Second word:



Extended addressing (op 00, M=6)

First word — A field splits in two:



Second word (address, or the operand if X=0-3):



Fn is the single-word instruction's own op/A-field code; X is the addressing-mode field, below.

Addressing Modes

M field — single-word instructions

M	Mode	Effective address
0-3	Direct	M bits 9-10 + A field: 11 bits, 0-2047
4	Relative	A field + (P+1): up to 512 ahead
5	Indexed X	A field + X register
6	Indexed B	A field + B register
7	Indirect	A field (0-511) names a pointer word

X field — extended instructions

X	Mode	Effective address
0-3	Immediate	Second word <i>is</i> the operand
4	Relative	Second word + (P+1)
5	Indexed X	Second word + X register
6	Indexed B	Second word + B register
7	Direct/Ind.	Second word's bit 15: 0 = direct address (15 bits, full 32K); 1 = indirect pointer

Indexing happens first, then indirection, so LDAE* addr, 2 indexes by B, then treats the result as a pointer.

Timing

- 1.8 μ s per machine cycle; each level of indirect addressing adds one cycle.
- Shifts: $1 + 0.147(n - 1)$ cycles for a count of n .
- Interrupts are taken only after a single-word instruction that isn't I/O, a shift, MUL/DIV, or an execute, and that didn't itself follow an I/O instruction (so a tight loop needs a NOP to be interruptible, two after an EXC).

Overflow (OF)

- Set by ADD/SUB on two's-complement overflow, and by INR/DCR at 077777/100000.
- Never cleared by arithmetic. ROF clears it; so does any jump, jump-and-mark, or execute whose *whole* tested condition is met and includes OF.

Front Panel & STEP Quick Facts

- U is the instruction register.** Every instruction is fetched into U before it runs. In STEP mode, U holds the *next* instruction and P points past it; STEP executes U.
- With **REPEAT** on, STEP executes U again without reloading it, only advancing P — how the bootstrap procedure enters a program a word at a time.
- HLT leaves itself in U:** after a halt, U still shows the HLT and P points to the next word. RUN resumes with a fetch from P.
- SYSTEM RESET** clears overflow, initializes every device, and makes the next STEP or RUN start with a fetch from P; it leaves A, B, X, and P alone.

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Instruction Set

Load / Store / Arithmetic / Logical

Mnem.	S-W	Imm.	Ext.	Operation
LDA	010000	LDAI	LDAE	(Y)→A
LDB	020000	LDBI	LDBE	(Y)→B
LDX	030000	LDXI	LDXE	(Y)→X
INR	040000	INRI	INRE	(Y)+1→Y
STA	050000	STAI	STAE	A→Y
STB	060000	STBI	STBE	B→Y
STX	070000	STXI	STXE	X→Y
ORA	110000	ORAI	ORAE	A OR (Y)→A
ADD	120000	ADDI	ADDE	A+(Y)→A
ERA	130000	ERAI	ERAE	A XOR (Y)→A
SUB	140000	SUBI	SUBE	A−(Y)→A
ANA	150000	ANAI	ANAE	A AND (Y)→A
MUL	160000	MULI	MULE	(A,B)×(Y)→(A,B)
DIV	170000	DIVI	DIVE	(A,B)÷(Y)→B, rem.→A

LDA/LOA (and every load) accept both spellings. Immediate/Extended base codes share one octal value with X (extended addressing) field 0 selecting immediate; see front page.

Jump / Jump-and-Mark / Execute

Base: JMP (M=1, jump), JMPM (M=2, store P at Y then jump to Y+1), XEC (M=3, execute the word at Y). Condition bits (A field, ORed):

OF	001	AZ	010	SS1	100
AP	002	BZ	020	SS2	200
AN	004	XZ	040	SS3	400

Named mnemonics for single conditions:
JOF/JAP/JAN/JAZ/JBZ/JXZ/JSS1/ JSS2/JSS3 (and JOFM... for mark, XOF... for execute). Multiple conditions: JIF cond,addr (JIFM, XIF).
Un-met condition: falls through (jump/mark) or is skipped (execute).

620/f “not” conditions (DAS MR)

JOFN, JANZ, JBNZ, JXNZ, JS1N-JS3N (+M mark, X execute forms): an ordinary condition field asking A to be both positive *and* negative, which a 620/f inverts and a 620/L never satisfies.

Shifts (M=4)

Mnem.	A field	Shifts
ASLB	0400+n	B left, A&B left (A,B linked)
LRLB	0000+n	B left, rotating
ASRB	0500+n	B right, A&B right (A,B linked)
LSRB	0100+n	B right, rotating
ASLA	0600+n	A left, A alone
LRLA	0200+n	A left, rotating, A alone
ASRA	0700+n	A right, A alone
LSRA	0300+n	A right, rotating, A alone
LASL	—	A,B linked left
LLRL	—	A,B linked left, rotating
LASR	—	A,B linked right
LLSR	—	A,B linked right, rotating

n = shift count, 0-31 (low 5 bits of A field).

Register Change (op 00, M=5)

Bits 0-8 of the A field, ORed freely:

Bit	Function
0	A is a destination
1	B is a destination
2	X is a destination
3	A is a source
4	B is a source
5	X is a source
6,7	Function: 00 transfer, 01 incr., 10 compl., 11 decr.
8	Perform only if OF is set (else unconditional)

Multiple sources OR together. Named combinations (octal A field):

NOP 0	no operation
TZA/TZB/TZX 1/2/4	clear A/B/X
TAB/TAX 012/014	A→B, A→X
TBA/TBX 021/024	B→A, B→X
TXA/TXB 041/042	X→A, X→B
IAR/IBR/IXR 111/122/144	increment A/B/X
DAR/DBR/DXR 311/322/344	decrement A/B/X
CPA/CPB/CPX 211/222/244	complement A/B/X

Control (op 00, M=7)

Mnem.	A field	Effect
ROF	0400	Clear overflow
SOF	0401	Set overflow
TSA	0402	Sense switches → A (620/f)
HLT	0 (all zero word)	Halt

Input/Output (op 10)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0															
10				Md				Fn				Device			
Md	Group			Mnemonics											
0	External Control			EXC, SEL											
1	Sense			SEN											
2	Input			IME, INA, INB, INAB, CIA, CIB, CIAB											
3	Output			OME, OAR, OBR, OAB											
4	Aux. Ext. Control			EXC2/SEL2 (also called EXCB)											

Fn (3 bits) selects the device’s function; Device (6 bits) addresses one of 64 devices. Meanings are per-device — see the peripheral’s own manual or v620emu’s docs/MANUAL.md.

MUL / DIV

- MUL: (A,B) × (Y) as a 31-bit result — A holds the sign and high 15 bits, B the low 15 (sign bit clear). −32768 × −32768 with A not negative overflows to zero.
- DIV: dividend in A,B (same layout); quotient→B, remainder→A with the dividend’s sign. OF set if the quotient doesn’t fit, or on divide by zero.
- 620/i and 620/L flaw (corrected on the 620/f): a negative dividend that divides evenly gives a quotient one too small and a remainder equal to the divisor’s magnitude, with the dividend’s sign.